REMARKS/ARGUMENTS

CLAIM INTERPRETATIONS

The Examiner stated at the end of paragraph 3, at the top of page 3 of the above-identified Office Action, that the Examiner interprets "slot" as being interchangeable with "system variable" in view of the Applicant's Specification at page 2, lines 10-15 and also at page 4, lines 1-3. Applicants appreciate the Examiner pointing out an ambiguity, which has been clarified by the above-listed amendment to the Specification. The language being amended above at page 2, lines 10-15 is in the Summary section, which was meant to summarize the more detailed description at page 4, lines 1-3.

In view of this amendment, Applicants respectfully request the Examiner to interpret the term "slot" as being NOT interchangeable with "system variable". Instead, the Examiner is respectfully requested to interpret these two terms as referring to two separate and distinct items that are related to one another by an association therebetween. Support for this interpretation is found throughout the originally-filed specification, including for example, page 5 lines 10-14 wherein the variable is referred to by one symbol (which is q'_j) and the slot is referred to by a different symbol (which is Q_j).

The Examiner also stated in paragraph 4, in the top half of page 3 of the above-identified Office Action, that the Examiner interprets the functionality of "simultaneous equations" to be equivalent to "simultaneous statements" as taught in IEEE Standard 1076.1-1999, March 18, 1999 (hereinafter simply "IEEE"). Applicants submit that the Examiner's interpretation is incorrect because simultaneous statements only define a subset of all simultaneous equations as per IEEE (see section 12.1, first paragraph, and section 12.6.5, 2nd paragraph)

Moreover, IEEE defines the concept of "characteristic expressions". As stated in the first statement in Section 15.1 in the middle of page 225 of IEEE, "The evaluation of a simple simultaneous statement creates one or more characteristic expressions of an explicit set." In the Applicants' description at page 4, line 20, the term "characteristic expression" is used as defined by VHDL-AMS, to be the set of simultaneous equations the simulator must solve at a given analog solution iteration. In contrast, Applicants note that Claim 1 does not use the term "characteristic expression." Instead, Claim 1 uses the term

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"conditional equation." As stated at page 4, lines 22-23, the term "conditional equation" is more general, and subsumes the term "characteristic expression."

Applicants have amended Claims 1 and 12 in accordance with the Examiner's suggestions in paragraphs 7 and 8 of the Office Action.

SPECIFICATION OBJECTION

Applicants address the Examiner's objection in paragraph 9 on page 4 of the above-identified Office Action by amendment to the specification at page 3. Specifically, the blank spaces are deleted and a reference is now made to a previous citation of the same patent application (at page 1). Accordingly, Applicants respectfully request the Examiner to withdraw the objection to the specification.

DOUBLE PATENTING REJECTION

Claims 1, 12, and 22 were rejected in paragraph 10 at the bottom of page 4 of the Office Action for double patenting over US Patent 6,532,569. The Examiner stated that the current claims require "selecting an active conditional equation" or "selecting a set of active conditional equations" while the claims of US Patent 6,532,569 which recite "classify an unclassified variable as an intermediate variable if the unclassified variable is defined by an equation."

Applicants submit that the Examiner has failed to make a prima facie case of obviousness of the current claims over the claims of US Patent 6,532,569, because the Examiner merely stated his/her final conclusion of double patenting at the bottom of page 4 of the Office Action. The Examiner has failed to make any factual determination of the type required by Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966). According to MPEP § 804 II (B) (1), a double patenting rejection of the obviousness-type is "analogous to [a failure to meet] the nonobviousness requirement of 35 U.S.C. 103" except that the patent principally underlying the double patenting rejection is not considered prior art. MPEP further states that any analysis employed in an obviousness-type double patenting rejection parallels the guidelines for analysis of a 35 U.S.C. 103 obviousness determination.

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Applicants further submit that the Examiner failed to follow the MPEP requirement that any obviousness-type double patenting rejection should make clear: (A) The differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application; and (B) The reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent." Regarding (A), the Examiner merely quoted language from the claims without any comparison whatsoever. Regarding (B), the Examiner was completely silent.

In considering the issue of double patenting, Applicants respectfully point out that the concept of an intermediate variable, which is used in Claim 18 of U.S. patent 6,532,569, is unrelated to conditional equations of the type recited in claims of the current patent application. Specifically, U.S. Patent 6,532,569 describes a methodology to classify quantities (as defined by IEEE) with the aim of reducing the number of system variables and therefore the number of equations needed to find a solution. One step of the reduction is the identification of a group of variables which in U.S. patent 6,532,569 are called intermediate variables. On the other hand, claims of the current patent application are related to how a set of simultaneous equations is formed if there are conditional equations. Note that the term "intermediate variable" is used in the "Background of the Invention" section of the current patent application (at page 1, lines 29-30). A reduction as described in U.S. Patent 6,532,569 is a useful prerequisite for methods of the type being claimed in the current patent application, but such reduction is not essential.

In view of the above, Applicants submit that the claims of U.S. Patent 6,532,569 are patentably distinct from the claims of the current patent application. Therefore, Applicants respectfully request the Examiner to withdraw the double patenting rejection.

§112 CLAIM REJECTIONS

Claims 1-23 were rejected in paragraph 13 on page 5 of the Office Action, as being not enabled in the specification. Specifically, the Examiner stated that "solving the system of simultaneous equations" is not described in sufficient detail for a skilled artisan to practice the invention.

Applicants submit that there is no connection whatsoever between the subject

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matter of the current patent application with the fields of integer programming and linear programming. Instead, a person of skill in the art, whose skill level is evidenced by IEEE cited by the Examiner, is presumed to know that "The base type of each simple expression must be the same natural type" as per IEEE (see section 15.1, p.225). A nature type is defined in IEEE (4.3.1.6, p.59) as "... a floating point type or a composite type whose elements are of a nature type." This clearly implies that IEEE is itself unrelated to integer programming. Therefore, anybody skilled in the art would also understand that the claimed invention of the current patent application is also unrelated to integer programming.

The current patent application describes in detail a specific methodology to prepare a set of simultaneous equations from (a) a collection of equations that do not change depending on the circumstances, and (b) another collection of equations that are conditional equations. As the Examiner correctly notes, the current patent application does not describe a specific methodology to solve the set of simultaneous equations, once prepared. No description of the solution is provided in the current patent application because the solution can be implemented using any conventional methodology for solving sets of simultaneous equations, so long as the sets are prepared in the manner described in the current patent application.

Applicants submit that the Examiner must take into account the level of skill in the art, including knowledge of many well known methodologies to solve sets of simultaneous equations. For example, the skilled artisan is presumed to be knowledgeable of methods described in basic text books, such as G. Dahlquist, A. Björk: "Numerical Methods", Prentice-Hall, 1974 and R. W. Hamming: "Numerical Methods for Scientists and Engineers", McGraw-Hill, 1962. The most famous method dates back to **Isaac Newton** and is commonly referred to as Newton's method. The Examiner cannot ignore the fact that Newton's method is taught in undergraduate courses on numerical mathematics. In view of the above, Applicants submit that any skilled artisan would immediately understand that any prior art method (**even Newton's method**) can be used to solve a set of simultaneous equations of the type prepared by the methodology being claimed.

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In this context, note that MPEP § 2164.08 states that not everything necessary to practice the invention need be disclosed. In fact, what is well-known is best omitted. ...

All that is necessary is that one skilled in the art be able to practice the claimed invention, given the level of knowledge and skill in the art. Further the scope of enablement must only bear a "reasonable correlation" to the scope of the claims. In view of the above, Applicants respectfully request the Examiner to withdraw the rejection for non-enablement of "solving the system of simultaneous equations."

Claims 22-23 were rejected in paragraph 14 at the bottom of page 5 of the Office Action, as being not enabled in the specification. The Examiner stated that "translation software" is not described in sufficient detail to practice the invention. The Examiner also stated that it was not clear to the Examiner if "translation" was equivalent to compilation, parsing, or other transformation of HDL code. The Examiner further stated that due to a large number of possible solutions, these claims would require undue experimentation.

Applicants submit that the detailed description of the current patent application cannot be any more precise than the language quoted by the Examiner (from page 8 lines 10-12), because the specific form onto which HDL code must be translated is different for each implementation. Some implementations may require a compilation while for others parsing may be sufficient. A specific translation that is to be done in a given implementation depends on the internal form in which the implementation represents the HDL code. The apparatus is being claimed in Claims 22 and 23 at a generic level, regardless of any internal form to which HDL code may be translated. As is well known in the art, there are many conventional methods which identify how HDL code is to be represented internally, depending on the implementation.

In fact, even the Examiner acknowledged that there are many conventional methods by stating "[g]iven the large number of possible solutions ..." (in the middle of page 6 of the Office Action). Hence, any single one of the "large number of possible solutions" acknowledged by the Examiner may be used to realize the benefits of the claimed invention. Therefore, Applicants submit that **no** experimentation is required to use an otherwise normally working apparatus, for solving simultaneous equations after being prepared as claimed. And preparation of the simultaneous equations has been amply illustrated and enabled in the detailed description of the current patent application. Thus Examiner's statement of undue experimentation is unfounded.

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Applicants further submit that the Examiner's statements of non-enablement are conclusory, without any basis whatsoever in the facts of the current patent application. The Examiner has completely ignored the following request made by Applicants in the prior Amendment:

> If the Examiner continues to make the enablement rejection, the Examiner must identify sufficient factual evidence to support a determination that a disclosure does not satisfy the enablement requirement and whether any experimentation that may be needed is "undue" based on the numerous factors specified in MPEP 2164.01 (a).

Specifically, the Examiner has failed to consider (and articulate in the above-identified Office Action) numerous factors identified in MPEP § 2164.01(a). These factors include, but are not limited to: (A) The breadth of the claims; (B) The nature of the invention; (C) The state of the prior art; (D) The level of one of ordinary skill; (E) The level of predictability in the art; (F) The amount of direction provided by the inventor; (G) The existence of working examples; and (H) The quantity of experimentation needed to make or use the invention based on the content of the disclosure.

If the Examiner continues to reject any claim for non-enablement, Applicants respectfully request the Examiner to state on the record what is the determination of each factor (A)-(H) for each rejected claim. The Examiner must also state the weight being given to each factor and provide a reasoned analysis for the final conclusion. As noted in MPEP § 2164.01, the determination that "undue experimentation" would have been needed to make and use the claimed invention is not a single, simple factual determination. Rather, it is a conclusion reached by weighing all the above noted factual considerations.

In paragraph 15 in the bottom half of page 6 of the Office Action, the Examiner rejected Claim 1 for omitting essential steps, citing to MPEP § 2172.01 and the second paragraph of §112. The Examiner's rejection is unclear, because omission of essential steps is stated in MPEP § 2172.01 as being rejectable under 35 U.S.C. §112, first paragraph (i.e. **not** second paragraph). In any case, Applicants respond below, assuming that the rejection was properly made under 35 U.S.C. §112, first paragraph.

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In explaining this rejection of Claim 1, the Examiner stated that none of the claim limitations reference simulation. The Examiner also stated that the final limitation references validation, but no mention is made as to how the solution is used to validate the system. Applicants submit that in the relevant literature, the term "simulation" or "computer simulation" is understood to mean finding the values of unknowns, such as system variables as a function of time. In this context, the values at a particular time are the solution of a set of simultaneous equations. Further, the term "validation" is understood to mean comparing these values over time with expected values that have been obtained using an alternative method, for example by a set of specifications. Applicants do not understand what additional steps the Examiner believes are required in Claim 1. Claim 1 already requires "solving the system of simultaneous equations" (which is understood to mean simulation), and Claim 1 also requires "using the solution ... to validate ..." (which is understood to mean comparison). If this rejection is continued, the Examiner is respectfully requested to identify a particular step the Examiner believes should be added to Claim 1.

Claims 2-23 were also rejected under the second paragraph of §112 in paragraph 16 at the bottom of page 6 of the Office Action. The Examiner stated that Claims 2, 12 and 22 omitted "final steps" after solving the system of equations at a current iteration. The Examiner stated that it wasn't clear when and how the final iteration was reached and what happens when reached.

As noted above in reference to Claim 1, numerous text books already discuss how a set of simultaneous equations is to be solved, once the set has been prepared. For this reason, Claims 2-23 do not prescribe a specific method to solve the set of simultaneous equations. Instead, Claims 2-23 only describe a methodology of how to prepare the set, in the context of conditional equations. After the set has been prepared, the specific implementation details of how the final iteration of a solution is reached, and what happens thereafter are irrelevant to the invention recited in Claims 2-23. Numerous methods that are currently known for the solution of simultaneous equations are iterative, and each of them has its own detail of how the final iteration is reached. Hence the §112 rejection of Claims 2-23 should be withdrawn.

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In this context, the Examiner is requested to bear in mind that MPEP § 2164.08(c) states that in determining whether an unclaimed feature is critical, the entire disclosure must be considered ... an enablement rejection based on the grounds that a disclosed critical limitation is missing from a claim should be made only when the language of the specification makes it clear that the limitation is critical for the invention to function as intended. Broad language in the disclosure, including the abstract, omitting an allegedly critical feature, tends to rebut the argument of criticality.

§101 CLAIM REJECTIONS

Claims 1-23 were rejected as being "not concrete or tangible ... because the claimed invention does not provide a concrete and tangible result..." The Examiner stated that the claims were directed to only the broad "solution to the system of simultaneous equations." The Examiner further cited examples of "telephone billing data, share price data, and pixel illumination intensity".

Applicants submit that Claim 1 requires a "solution" of the system of equations as its intermediate step. Claim 1 does require a last step to "validate the physical circuit or system." Applicants submit that validation of the physical circuit or system is a tangible result, because the circuit designer has gained valuable knowledge, that their physical circuit has been validated. As would be apparent to the skilled artisan, validation of a physical circuit is commercially valuable and tangible result. The result (that a circuit design has been validated) is frequently recorded and reported by circuit designers, and the result is even accepted and relied upon by fabs in subsequent manufacture of integrated circuits (ICs). Thus the validation result of Claim 1 is analogous to a final share price, which is recorded and reported and accepted and relied upon by regulatory authorities and in subsequent trades, as per State Street, 149 F.3d at 1373, 47 USPQ2d at 1601. The last step to "validate the physical circuit or system" is explicitly recited in Claim 1 and cannot be ignored by the Examiner.

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In this context, Applicants also respectfully request the Examiner to further consider that Claim 1 requires "representing the physical circuit ... as a system of simultaneous equations." This representation step of Claim 1 is believed to provide additional support for the patentability of Claim 1.

Finally, Claim 1 has now been amended to recite that each of the claimed steps is performed inside a computer. In view of the above, Applicants are not seeking to patent an idea in the abstract, a law of nature or a natural phenomenon. Instead, Claim 1 is clearly drawn to a real-world process performed in a real-world computer. Therefore, the rejection of Claim 1 for reciting non-statutory subject matter should be withdrawn.

Claims 2-21 have also been amended to recite that each of the claimed steps is performed in a computer. Therefore, the rejection of Claims 2-21 for reciting non-statutory subject matter should also be withdrawn. Note further that Claim 9 requires "reporting a simulation failure" which provides an independent ground for withdrawal of the non-statutory subject matter rejection.

Furthermore, Claim 22 already recites a computer and related software and means, all of which are well established as being real-world devices worthy of patent protection under the current law. Accordingly, Applicants respectfully request the Examiner to withdraw the non-statutory subject matter rejection of Claims 22 and 23.

Finally, Claims 2-23 were also rejected for lacking utility. The Examiner stated that it was not clear what useful benefit is derived from solution of equations. In response, Applicants respectfully direct the Examiner's attention to page 7, lines 13-16, wherein the result of solution is described as being useful in (a) a next iteration or (b) to validate the physical circuit or system. In view of these two explicitly recited utilities, Applicants submit that a solution resulting from Claims 2-23 does have one of these two utilities. Therefore, the rejection of Claims 2-23 for not having utility should be withdrawn.

LACK OF PRIOR ART

Applicants note that the Examiner has expressly acknowledged the lack of prior art to reject the current claims, in the bottom half of page 10 of the Office Action as follows:

> ... Examiner has not been able to find a reference that teaches dynamic scheduling of analog equations with IEEE Std 1076.1-1999 (also called VHDL-AMS) and that also pre-dates the priority filing date of this application

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In view of the above-quoted remark, Applicants are entitled to broad claims, commensurate with originally-filed disclosure. In view of the lack of prior art, the Examiner is respectfully requested to not unnecessarily limit Applicants claims, under §112 or §101. To the extent any genuine issues continue to exist with the specific language of any claim, such issues may be resolved via a verbal discussion. Hence, Applicants strongly urge the Examiner to call the undersigned, so that prosecution on the merits can be closed, if appropriate, by an Examiner's Amendment.

In closing, Applicants respectfully request allowance of all Claims 1-23. As noted above, the Examiner is invited to call the undersigned at (408) 982-8200, ext. 3 if there are any questions whatsoever.

Via Express Mail Label No.:

EV 448 867 189 US

Respectfully submitted,

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